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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,999	11/21/2003	Knut Kahlisch	1890-0011	1506

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EXAMINER

RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11A

<b>Office Action Summary</b>	<b>Application No.</b> 10/719,999	<b>Applicant(s)</b> KAHLISCH ET AL.	
	<b>Examiner</b> Steven H. Rao	<b>Art Unit</b> 2814	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11, 13, 14 and 23-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-11, 13, 14 23-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Priority***

Acknowledgement is made of papers filed under 37 CFR 1.114 claiming priority from U.S. Serial No. 10/719,999 filed on November 21, 2003 which itself claims priority from German Patent Application No. 1025648.7 filed on November 22, 2002.

### ***Preliminary Amendment***

Applicants' amendment filed on August 08, 2005 along with the RCE request has been entered and forwarded to the Examiner on August 16, 2005.

Therefore claims 1-11, 13-14 as amended and claims 23 to 31 presently newly added are currently pending in the Application.

Claims 16-22 have been cancelled.

### ***Information Disclosure Statement***

No further IDS after the one filed on October 18, 2004 has been filed in this case.

The IDS filed on October 14, 2003 has been entered on October 18, 2004.

An initialed copy of the PTO-1449 dated October 14, 2003 ( and also resubmitted May 04, 2005) was previously enclosed with the Final rejection mailed on May 04, 2005 .

### ***Claim Rejections - 35 USC Section 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

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matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-11 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. ( U.S. Patent Application publication No. 2002/0092162 now USP No. 6,772,512, herein after Tsai) in view of Kovac ( U.S. Patent No. ) With respect to claim 1, to the extent understood, Tsai describes a package supporting structure for a chip, comprising: a supporting substrate with a bond opening therein (Tsai figure 2A # 210-substrate , opening # p, Kovac figures 2-3.#10 with opening 16, col. 3 lines 60-67) ; an interconnect layer on the supporting substrate Tsai figure 2 B # 221, Kovac figure 4 # 12) in which a bonding channel overlapping with the bond opening is formed, ( Tsai figure 2B-C, # 21 1 etc. Kovac col. 4 lines 4-6, not illustrated in figures) and a chip mechanically fixed to the interconnect layer to cover the bonding channel ( Tsai figure 2 B 220 ) an encapsulation material arranged in the bonding channel ( Tsai col. 5 lines 5-7) an escape prevention structure for the bonding channel, ( Kovac figure 4 # 26,30) to enable escaping of air from the bonding channel and to substantially prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure.

The recitation, " to enable escaping of air from bonding channel and to substantially prevent the encapsulation material from escaping from the bonding

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channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure." are taken to be functionally inherent properties.

It is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter, may in fact be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. In re Swinehart 169 USPQ 226 (CCPA 1970).

( It is noted that Tsai col.3 lines 5-10, col. 5 lines 10-13 Kovac figure 4, etc. and abstract lines 2-12 describe the functionally inherent property to enable escaping of air from bonding channel and to prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure ).

With respect to claim 2 the package of claim 1 wherein the escape prevention structure is designed to prevent escaping of the Kovac describes the supporting structure of claim 1 lines 50-54), encapsulation material due to the capillary effect. ( Kovac col. 4

With respect to claims 3 and 4 Kovac describes the package of claim 1, wherein the escape prevention structure includes an opening with such a

cross-sectional area, so that escaping of the encapsulation material caused by the capillary effect is prevented. ( Kovac's Abstract last 6 lines, col.4 lines 50-54 and figures 1-5 ,etc.).

With respect to claim 5 Kovac describes the package (supporting structure ) of claim 4, wherein the barrier structure is connected to the interconnect layer. ( Kovac col. 4 lines 17- 18).

With respect to claim 6 Kovac describes the package (supporting structure ) of claim 4, wherein tie barrier structure is formed integrally with the interconnect layer. ( Kovac figures 30 and 32 formed integrally).

With respect to claim 7 Kovac describes the ( package) supporting structure of claim 4, wherein the barrier structure extends across the entire width of the bonding channel. ( Kovac e.g. figure 4 30 extends across wider portion above 20).

With respect to claim 8 Kovac describes the ( package) supporting structure of claim 4, wherein the barrier structure is formed, so that a cross-section of the bonding channel tapers in a direction to the lateral end. (Tsai figure 1B) .

With respect to claim 9 Kovac describes the ( package) supporting structure of claim 4, wherein the barrier structure has a convex shape. ( Tsai fig. IB #140).

With respect to claim 10 Kovac describes the ( package) supporting structure of barrier structure is disposed in the bonding channel and spaced from the interconnect layer. (Kovac e.g. figure 4 , 30 disposed in 14, 20 spaced ffrom 32).

With respect to claim 11 Kovac describes the ( package) supporting structure of

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claim 4, wherein the supporting structure of the escape prevention structure includes a recess in the supporting substrate ( Kovac figure 4 # 20).

With respect to claim 13 Kovac describes the ( package) supporting structure of claim 1 1 , wherein the interconnect layer is disposed on a surface of the supporting substrate, wherein the recess on the surface extends across a sidewall of the bonding channel. (Kovac figure 3 , 32 on surface of 12, recess 20 along side wall of bonding channel).

With respect to claim 14 Kovac describes the ( package) supporting structure of claim 1 1 , wherein the recess is disposed in a region of the bonding channel, wherein the recess extends from a first surface of the supporting substrate to a second surface of the supporting substrate. ( Kovac figure 4 recess extends form top to bottom surface of support substrate 12).

Presently newly added claims :

With respect to claim 23 Tsai describes an arrangement for use in a package, comprising : a supporting substrate with a bond opening therein; ( tsai figure 2A # 210- substrate , opening #p, Kovac fis. 2-3 #10 with opening 16, col. 3 lines 60-67) an interconnect layer disposed on the supporting substrate ( Tsai fig. 2 B # 221, Kovac fig. 4 # 12 ) a bonding channel overlapping with the bond opening disposed in the interconnect layer; ( Tsai figure 2B\_C # 211 etc. Kovac col. 4 lines 4-6, not illustrated in figures) a chip fixedly secured to the interconnect layer and substantially covering the bonding channel; ( Tsai figure 2 B #220) an encapsulation material arranged in the bonding channel; ( Tsai col. 5 lines 5-7) and an escape prevention structure disposed

between the chip and the supporting substrate, ( Tsai figs. 2 D, F and Kovac fig. 4 # 26, 30) the escape prevention structure configured to substantially prevent an encapsulation material flow out of the bonding channel, and further configured to enable escaping of air from the bonding channel.

The recitation, " to enable escaping of air from bonding channel and to substantially prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure." are taken to be functionally inherent properties.

It is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art , does not cause a claim drawn to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing, novelty in the claimed subject matter , may in fact be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. In re Swinehart 169 USPQ 226 (CCPA 1970).

( It is noted that Tsai col.3 lines 5-10 , col. 5 lines 10-13 Kovac figure 4, etc. and abstract lines 2-12 describe the functionally inherent property to enable escaping of air from bonding channel and to prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure ).



With respect to claim 24 Tsai describes the arrangement of claim 23, wherein the bonding channel has an opening at a lateral end, and wherein the escape prevention structure defines the cross section of the opening of the bonding channel. ( Tsai, Kovac figures)

With respect to Claim 25 Tsai describes the arrangement of claim 24, wherein the escape prevention structure includes a portion connected to the interconnect layer. ( Kovac col.4 lines 17-18).

With respect to claim 26 Tsai describes the arrangement of claim 24, wherein the escape prevention structure includes a portion formed integrally with the interconnect layer. Kovac col.4 lines 17-18).

With respect to claim 27 Tsai describes the arrangement of claim 24, wherein the escape prevention structure includes a portion that extends across the entire width of the bonding channel. ( Kovac e.g. figure 4 , 30 extends across wider portion above 20)

With respect to claim 28 Tsai describes the arrangement of claim 24, wherein the escape prevention structure is formed such that a cross-section of the bonding channel tapers in a direction to the lateral end. ( Tsai figure 1 B).

With respect to claim 29 Tsai describes the arrangement of claim 24, wherein the escape prevention structure has a convex shape.( tsai figure 1 B #140).

With respect to Claim 30 Tsai describes the arrangement of claim 24, wherein the escape prevention structure is disposed in the bonding channel and spaced from the interconnect layer.( rejected for reasons set out under claim 10 above)

With respect to claim 31 describes the arrangement of claim 24, wherein the escape prevention structure includes a recess in the supporting substrate. ( rejected for reasons set out under claim 11 above).

### ***Response to Arguments***

Applicant's arguments filed on 08/08/2005 have been fully considered but they are not persuasive for the following reasons :

Applicants' contention that, "One of ordinary skill in the art would not modify Tsai to substantially prevent encapsulation material from flowing outside of a bonding channel that is located in its ball grid array "layer" because it would defeat the purpose of Tsai to encapsulate the entire chip, including portions external to the ball grid array." Is not persuasive because the above conclusion is based on incomplete understanding/analysis of the applied Tsai reference .

The Tsai reference , itself teaches that

During a molding process, when the encapsulation material infiltrates to the exit of the vent hole, it can be confined within the groove in the elevated flat surface over the dummy pad, thereby preventing it from flashing to nearby solder-ball pads. Since there would substantially exist no mold flash over the exposed surface of the solder mask and the solder-ball pads, the proposed method allows the resulting FCBGA package to be assured in the quality of its outer appearance and the quality of the electrical bonding between the solder-ball pads and the subsequently attached solder balls thereon to make the encapsulated semiconductor chip reliable to use during operation.

( abstract last 12 lines) .

and an important problem solved by Tsai is described in col. 2 lines 44 to 54 ( reproduced below).

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One problem to the foregoing molded-underfill process, however, is that the encapsulation material would further infiltrate all the way through the vent hole 111 to the recessed portion 140b of the solder mask 140 (the marching path is indicated by the arrows in FIG. 1B); and after filling up the recessed portion 140b of the solder mask 140, the encapsulation material would further infiltrate through the seam between the molding tool 170 and the bulged portion 140a of the solder mask 140 to the nearby solder-ball pads 130, thus causing mold flash 151 over the solder-ball pads 130.

From the above it will be very clear to one of ordinary skill in the art that a complete reading/analysis of Tsai must include the fact that Tsai wants to prevent the encapsulant material from randomly flowing in the under fill and contacting with 130 as shown in figures 1 B and D (describing prior art figures ) and shown as 151 in these figures which result in mold flash.

Therefore Tsai teaches a very specific path ( confined within the groove ) for the encapsulant to flow e.g. by introducing element 231 ( dummy pad ) and 241 ( elevated

During a molding process, when the encapsulation material infiltrates to the exit of the vent hole, it can be confined within the groove in the elevated flat surface over the dummy pad, thereby preventing it from flashing to nearby solder-ball pads. Since there would substantially exist no flat surface)

Therefore Tsai teaches a very specific path ( confined within the groove) for the encapsulant to flow and achieves the encapsulation of the entire chip without the encapsulant material coming into contact with the solder balls e.g. 130 and thereby preventing mold flash by the presence of additional elements e.g. element 231 ( dummy pad ) and 241 ( elevated flat surface) one of ordinary skill armed with the teachings of Tsai to confine the encapsulant flow within groove by the presence of additional elements e.g. element 231 ( dummy pad ) and 241 ( elevated flat surface) to e.g. prevent mold flash (i.e. prevent the encapsulant from coming in to contact with .eg.

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solder balls 130 ) while encapsulating the entire chip would be motivated to find substitute other escape prevention structures that enable escaping of air from bonding channel and to prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure , i.e. provide a very specific path ( confined within the groove) for the encapsulant to flow.

Therefore Applicants' argument is not persuasive.

Dependent claims 2-11, 13, 14 and 23-31 were alleged to be allowable because of their dependency from allegedly allowable claim 1 and similar reasons as those stated under claim 1 above .

However, for reasons set out under claim 1 above , those reason/s are not persuasive and claims 2-11,13,14 and 23-31 are also rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is ( 571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

A handwritten signature, possibly reading "Rao", is located at the bottom right of the page.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven H. Rao

Patent Examiner

October 13, 2005.



LONG PHAM  
PRIMARY EXAMINER